Dan I. Hariton
http://www.danhariton.com/
Cellular Phone **1-408-981-4788**
Email_ID: **dan@danhariton.com**

Objectives

Analog and Digital, Mixed Signal IC definition, design, system integration, project management. Provide technical guidance and consulting. Design and manage, extend expertise and success methods to design groups. Interpersonal commitment to design methods, discipline, and communication. Patent new design ideas at the rate of one per year or more.

Consulting 2009 – Present

- D_Link DHP301 AC line communications: HD200 data throughput evaluation with AC impulse and noise
- Solar power conversion: Power injection into residential and industrial power grids
- Gyro dynamics study: Conversion of torque to linear acceleration

PulseCore Semiconductor, Inc. 2000 to 2008

- IC design: mixed-mode analog(amplifiers, bandgaps, comparators, mixers, PLLs, crystal oscillators) and digital (FFs, transmission gates, fractional counters, ROM memory, I/O blocks, delay lines), LDO PWM SMPS IC and architecture
- PLL Specific Designs: spread spectrum generation/modulation with jitter preservation (patent pending), zero I/O delay, C++ fractional_N counters, zero-cycle slip, device, block, and system level simulation HSPICE PVT, MatLab, C++, LINUX OS, PC and SUN platforms
- Process selection and IC design: CMOS 0.35um, 0.25um, CMOS_HV (20v, 40v), BiCMOS and bipolar
- Characterization of IC prototype PCBs with integrated and discrete components, indigenous and competitive IC evaluation/studies, PVT functional proof and characterization of IC critical parameters
- **USB2.0 Spread Spectrum IC**: **Industry's First** Demonstrated architecture and functionality (proof of concept) in MatLab and Simulink (Time domain and Frequency domain). Defined frequency generation maps for single universal-and-versatile SSC IC (12-24-30-48MHz seed clock). Generated all details block diagrams for design group. Reviewed design, special MR requirements, initiated ECR for xtal oscillator improvement. Reviewed characterization reports.
- USB2.0 specification analysis for SSC. Tektronix, USB-IF, HW & SW LAB compliance testing.
- **SATA, HDMI, FireWire**, specification study for SSC IC design
- Concurrently demonstrated USB2.0 compliance and 10m radiated EMI reduction of -4dB at 480MHz.
- Concurrently demonstrated USB2.0 functionality and 10m EMI reduction of -12dB at 480MHz
- **PCC024_ASM1800 PWM SMPS IC design**: spread-spectrum PWM switch-mode IC. Generic PWM controller with spread spectrum and fundamental attenuation. PWM+SS Modulator, Fixed and adaptive retiming, MatLab simulations, harmonic optimization, and patent applications. **Industry's First**, January_2003_Yahoo!_Finance: Alliance Semiconductor Tackles EMI -Reduction in Switching Power Supply Market
- **HIGH_VOLTAGE W40 PWM SMPS IC** ATMEL Fab and Austria Microsys: Managed design group, four IC designers, die size projection, maintain same pin compatibility with 384x, non_PLL SS generation, MatLab simulations, fundamental SS suppression, INDIA co-design review. LDO design.
- Co invented **Timing-Safe SSC Family of ICs** (Zero Cycle Slip). Patented architecture, **Industry's First**
- **PC31A ADC+SS_PLL+FIFO** Managed design group, 3 IC designers, 2 mask designers, UMC tapeout 6 weeks, all blocks functional, post-tapeout LVS clean, new process, new IC architecture
- **ZDB W34 and PCC028** original design and library blocks, on-chip SS generation (patent), design sent and expanded in INDIA for multipurpose ZDB SSC ICs. Design reviews, simulations, conference calls, engineering characterization, ESD
- **W36 P2779 APPLE IPOD and BANTAM** Low-current power budget calculation for clock+SS for consumer MP3 players
- **IMP SUPERVISORY** Technology assessment and transfer to INDIA. ESD, yield improvement, schematics review
- **PC2781-2-4** Mixed signal analog and digital SSC IC design |Fin-Fout|<1Hz. MOSIS CMOS 0.35um TSMC process. MATLAB and SIMULINK top level PLL system architecture for spread-spectrum 287x. C++ programming and design of lockup-free fractional modulo counters.
- PLL design verification and VCO range extension 70MHz - 600MHz
- All digital DLL wide range 20 MHz to 160 MHz
- Crystal oscillator design, guaranteed start-up over PVT
- Rail-to-rail I/O operational amplifier (5MHz, 100dB, 200uA)
- Patent for capacitor size reduction (Impedance Emulator)

Cellular Phone **1-408-981-4788**
Email_ID: **dan@danhariton.com**

Capella Microsystems, Inc. 1998 to 2000

- RC parasitic, and noise reduction
- Mixed signal IC design for CD_R, DVD_R laser signal pick-up TSMC CMOS 0.35um technology
- Photodiode front-end trans-impedance amplifier, 100-140MHz patented architecture
- Functional silicon 120MHz
- Patented TIA architecture "BIST for testing a current-voltage conversion amplifier"

National Semiconductor Inc. 1993 to 1998 and 1988 to 1990

LAN Group

- 100MHz Physical Layer IC design ("Phyter," 0.5um CMOS, IC functional at 135m CAT5 cable): 30MHz 8-bit segmented D/A for base-line wander compensation loop (design completed in 2 months). 30MHz 8-bit binary weighted D/A for peak tracking and data slicing (design completed in 2 months). 2,5GHz (static, Idd<2mA) comparator for peak tracking and data slicing (design completed in 2 months). Provided design guidance to junior engineers. Published several internal MOS design guides. Made functional 100Mbps, twisted-pair, transceiver IC "Twister".
- Extensive microscope-station work, silicon-die probing, and device-matching analysis, layout-and-circuit-design failure analysis for yield improvement.

LINEAR Group

- Flat-panel column driver 0.8um CMOS IC development: LMC7503 I LMC7504. IC functional.
- Activities included: specification development, mixed-mode simulation, NEXCELL, trace delay calculation / simulation, prototype evaluation, test development and microscope probing, test equipment, hardware and software acquisition, power dissipation reduction to suit customer requirements, automatic layout synthesis LAS - CADENCE.
- GIFT - Intelligent Battery Project: crystal oscillator study, results and recommendations.
- LM324 redesign for SOI integration: pattern layout and evaluation for compatibility with bonded-wafer / SOI technology.
- Infrared photodiode receiver for IrDA - open air - transmission: development study.
- Team leader and facilitation skills training.

CLASIC Group

- Bipolar designs. Full-custom, mixed-mode ICs. Voltage Regulator. 50% design. Loop stability.
- Liquid Analyzer. V-to-F converter. 100% design (0.5% linearity error) with 16 channels multiplexer. Under-Voltage detector, 100% design Actuator-Predriver. 10% design. Cell layout verification, routed the cell interconnections. Verified the full IC layout. Used in the IBM System 6000 workstation disk-drive. Gate-Channel LSI. 50% design. R&D project. Extensive, full system, SPICE simulations (800 bipolar transistors). Average pulse pairing was 1.2nsec. Blind assembly yield was > 50% (50 ICs, 30 functional).
- Motor Control. 100% design. Layout completed.
- Low-Noise, Gain-Controlled Amplifier. 80dB range, low DC shift, state-of-the-art IC. 100% design for medical ultrasound imaging. Low-voltage, gain-controlled, audio amplifier. 1.8 volts supply, LOG response, 60dB range. 100% design.
- Supervised 3 design engineers. Project management and performance reviews.

Silicon Systems Inc. 1991 to 1993

- Mixed-mode disk-drive IC functions. Logic design and verification of a serial-to-parallel decoder. Added adjustable delay to the clock and time channel while maintaining constant the group delay.
- Low-noise RW front-end IC design and failure analysis (0.4nV/Hz^0.5)

Consulting 1988 through 1991

- Project: 0.92GHz RF transmitter +24dBm. High-frequency section designed in 100 hours (oscillator, buffer, mixer, power amplifier). PSPICE 5.0 tools, Bipolar process.
- Project: Photodiode amplifier, HP2200 second source. Bipolar process.
- Project: Bipolar, l6-channel, neutron impulse detector. Nine circuit blocks: input amplifier, l6-to-1 analog combiner, address logic (comparators, 200mV differential ECL latches, TTL outputs), 4-bit flash A/D converter with latched outputs, set-reset logic, 16-to-4 A/D decoding logic, dynamic-bias gates, IPTAT and

ICONST current regulators. 80% utilization of an existing bipolar array with 2400 NPN-only transistors.

- Project: Systems, Power-line communications, FCC Part 15, UL and VDA safety guidelines, field trials. Security System to monitor the electronic locks of hotel doors. Power line transmission survey of the Hyatt O'Hare Airport hotel in Chicago. The survey results contributed to beta site installation and monitoring of electronic lock status in Hyatt O'Hare guest rooms.

Patent Applications in Progress

20090028218	USB system with spread spectrum EMI reduction US and PCT/International/ Applications
20070159744	High voltage pin for low voltage process
Unpublished	Zero Delay Buffer with Spread Spectrum (ZDB+SS) and Zero Cycle Slip (ZCS). FIFO depth calculation continuation-in-part

Granted Patents

1	7,679,464	Method and apparatus for frequency modulating a periodic signal of varying duty cycle Non-PLL
2	7,676,012	Spread spectrum controllable delay clock buffer with zero cycle slip
3	7,561,002	Method and apparatus for frequency modulating a periodic signal of varying duty cycle
4	6,646,463	Impedance emulator Non-Miller capacitance multiplication
5	6,624,405	BIST for testing a current-voltage conversion amplifier Transimpedance amplifier
6	6,351,137	Impedance emulator Non-Miller capacitance multiplication
7	6,104,588	Low noise electrostatic discharge protection circuit for mixed signal CMOS integrated circuits
8	5,926,064	Floating MOS capacitor Mentioned in "CMOS Mixed-Signal Circuit Design" R. Jacob Baker
9	5,920,232	Compensated, bias-dependent signal filter and amplifier circuit
10	4,845,466	System for high speed digital transmission in repetitive noise environment Time-hopping

Customer Testimonials

- PulseCore Semiconductor Taps Tektronix USB Serial Test Suite to Achieve Industry First. 2008 http://www2.tek.com/cmswpt/prdetails.lotr?ct=PR&cs=nwr&ci=14277&lc=EN
- PulseCore Semiconductor Turns to Tektronix USB Test Solution and Spectrum Analyzers to Enable USB2.0 Chip Development. 2008 http://www2.tek.com/cmsreplive/pmrep/14239/46W_23020_1_2008.09.30.11.19.28_14239_EN.pdf
- PulseCore Semiconductor pushes EMI suppression boundaries with Ellisys. 2008 http://www.ellisys.com/technology/customer_pulsecore.pdf

Education

UC Berkeley IC design classes: Data Conversion (X236, X237) --2010, MOS and bipolar IC circuit design, C++ Programming, classes in telecommunications
Bucharest Polytechnic MSEE

Selected Publications

A Commodity Analog Process Based on Bonded Wafers by K. McStay, F. Smoot, D. Hariton, K. Egan, D. Irvine, G. Brown, P. Edwards, S. Blackstone, H. Gamble. Proceedings of the 3rd International Symposium on Semiconductor Wafer Bonding: Physics and Applications, vo1.95-7, pp.466-470, ISBN 1-56677-101-3, Electrochemical Society, Reno, Nevada, May 21-26,1995.
A 240 Output, 64 Gray scale, TFT AM-LCD Column Driver by P. T. Wong, M. Huda, B. J. Shanker, C. Williams, D. Hariton. NSC proceedings of the lst International Technology & Innovation Conference, pp. 107-110, Santa Clara Marriott, April 10-13,1995.
Crystal Oscillator for the Intelligent-Battery Project, GIFT by Dan Hariton NSC_AMPS internal report, 100 pages, Santa Clara, 9-25-1995.
Layout Synthesis Evaluation Report by Dan Hariton, James Lu, Maq Mannan, John Pierce, Debbie Kitani, NSC internal report, pp.12-19, 11-8-1993.